

**IN THE CLAIMS:**

1-15. Canceled

16. (Currently Amended) A sub-micron MOS transistor comprising:  
a substrate; and  
an active region, including a gate region having a length of less than one micron; a source region including a LDD source region; and a drain region including a LDD drain region; wherein the ion concentration in said source region and in said drain region is between about  $1 \cdot 10^{20} \text{ cm}^{-3}$  to  $1 \cdot 10^{21} \text{ cm}^{-3}$ , and wherein the ion concentration in said LDD source region and in said LDD drain region is between about  $1 \cdot 10^{19}$   ~~$5 \cdot 10^{18}$~~   $\text{cm}^{-3}$  to  $5 \cdot 10^{19} \text{ cm}^{-3}$ .

17. (Original) The MOS transistor of claim 16 which further includes an insulating oxide layer thereover and a source electrode, a gate electrode and a drain electrode.

18. (New) A sub-micron MOS transistor comprising:  
a substrate; and  
an active region, including a gate region having a length of about 100 nanometers; a source region including a LDD source region; and a drain region including a LDD drain region; wherein the ion concentration in said source region and in said drain region is between about  $1 \cdot 10^{20} \text{ cm}^{-3}$  to  $1 \cdot 10^{21} \text{ cm}^{-3}$ , and wherein the ion concentration in said LDD source region and in said LDD drain region is between about  $5 \cdot 10^{18} \text{ cm}^{-3}$  to  $5 \cdot 10^{19} \text{ cm}^{-3}$ .

19. (New) The MOS transistor of claim 18 further comprising:

- a gate oxide layer overlying the active region;
- a source electrode;
- a gate electrode; and
- a drain electrode.

20. (New) A sub-micron MOS transistor comprising:  
a substrate;

an active region, including a gate region having a length of less than one micron; a source region including a LDD source region; and a drain region including a LDD drain region; wherein the ion concentration in said source region and in said drain region is between about  $1 \cdot 10^{20} \text{ cm}^{-3}$  to  $1 \cdot 10^{21} \text{ cm}^{-3}$ , and wherein the ion concentration in said LDD source region and in said LDD drain region is between about  $5 \cdot 10^{18} \text{ cm}^{-3}$  to  $5 \cdot 10^{19} \text{ cm}^{-3}$ ; and

a gate oxide layer overlying the gate region having a length about twice as long as the gate region length.

21. (New) The MOS transistor of claim 20 further comprising:

- a source electrode;
- a drain electrode; and
- a gate electrode having a length about half the length of the gate oxide layer.